MSLIN-98-001

Gau-2811

Surler #2/IDS 11/5/98


September 6, 1998

To: Commissioner of Patents and Trademarks
Washington, D.C. 20231

Fr: George O. Saile, Reg. No. 19,572
20 McIntosh Drive
Poughkeepsie, N.Y. 12603

Subject: Serial No. 09/131,429 08/10/98

M.S. Lin

WAFER SCALE PACKAGING SCHEME

Grp. Art Unit: 2811

INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty of disclosure under CFR 1.97-1.99 and 37 CFR 1.56. Copies of each document is included herewith.

Each of these following Patents and/or Publications have been mentioned and described in the Specification of the Subject Patent Application:

Recently, wafer scale packagaing has been gaining popularity. By this we mean that the entire wafer is packaged prior to its being separated into individual chips. A good example of this has been in a recent publication by M. Hou, "Wafer level packaging for CSPs", in Semiconductor International, July 1998, pp. 305-308.

Sincerely,

George O. Saile, Reg. No. 19572